REMARKS

Present Status of the Application

The Office Action mailed on Septembet 22nd, 2004 rejected all presently-pending claims 1-23. Specifically, the Office Action rejected claims 1-23 under 35 U.S.C. 103(a), as being unpatentable over Wieczorek et al. (U.S. 2004/0121565). Applicants have amended claims 1, 8 and 14, canceled claims 2-4, 9-11, 15-20 and 23 and added claims 24-31 to improve clarity. No new matter has been added to the application by the amendments made to the claims, specification or otherwise in the application. After entry of the foregoing amendments, claims 1, 5-8, 12-14, 21-22 and 24-31 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The Applicants' invention is directed to a method for manufacturing a metal-oxide-semiconductor transistor. In the present invention, a BTBAS (Bis(tert-butylamino)silane) is used as a precursor to carry out the deposition of the dielectric layer for forming a second spacer.on the substrate aside a first spacer formed on the sidewall of a gate structure. Because the formation condition, such as the deposition temperature, of the second spacer is suitable for performing solid phase epitaxial process to re-crystallize the amorphized material, **the re-crystallization process for the amorphized gate and the amorphized portion of the substrate can be performed while the second spacer is formed**. Further, **the activation of the**

dopants in the source/drain extension region in the substrate formed before the spacer is formed can be performed together with the formation of the second spacer. Therefore, the sheet resistance of the formed source/drain extension region can be greatly reduced and the problem of relatively high sheet resistance at the source/drain region and the relatively low saturated drain current can be overcome.

Discussion of Office Action Rejections

The Office Action rejected claims 1 23 under 35 U.S.C. 103(a), as being unpatentable over Wieczorek et al. (U.S. 2004/0121565) and stated that

> ".....Wieczorek discloses most of the steps of claimed invention but fails to disclose the step of forming a first spacer before forming doped source/drain extension region. However, it is conventional in the art that spacer is formed to obtain lightly doped extension regions, and it is obvious that the device would yield the same functions, results having with or without spacer when forming extension regions......"

Applicants respectfully traverse the rejections but has amended claims 1, 8 and 14 to clearly define the method according to the invention. As amended, claims 1, 8 and 14 recite:

> *1. A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:*
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> ....
>
> ***forming a second spacer on the sidewall of the first spacer, meanwhile, performing a solid phase epitaxial process to re-crystallize the amorphized conductive layer in the gate structure and activating a plurality of first dopants in the doped source/drain extension region;*** *and*
>
> *forming a doped source/drain region in the substrate on each side of the second spacer.*

> *8. A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:*
>
> *…………*
>
> ***forming a second spacer on the sidewall of the first spacer, meanwhile, performing a solid phase exitaxial process to re-crystallize the amorphized portion of the substrate and activating the doped source/drain extension region****; and*
>
> *forming a doped source/drain region in the substrate on each side of the second spacer.*
>
> *14. (currently amended) A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:*
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> *providing a substrate having a gate structure formed thereon, wherein the gate structure includes a gate insulating layer formed on the substrate, an amorphized gate formed on the gate insulating layer and a first pacer formed on a sidewall constructed by the gate insulating layer and the amorphized gate, and a portion of the substrate uncovered by the gate structure has been amorphized;*
>
> *…………*
>
> ***forming a second spacer on the sidewall of the first spacer, meanwhile, performing a solid phase epitaxial process to re-crystallize the amorphized gate and the amorphized portion of the substrate and activating a plurality of first dopants in the doped source/drain extension region****; and*
>
> *forming a doped source/drain region in the substrate on each side of the second spacer.*

(*Emphasis Added*). Applicants submit that each of these claims patently defines over the prior art of record, for at least the reason that the prior arts fail to disclose at least these elements emphasized above.

Applicants emphasize that the formation of the second spacer, the re-crystallization of the amorphized gate/substrate and activation of the source/drain extension region can be performed by a single process since by using a BTBAS (Bis(tert-butylamino)silane) as a precursor to form a dielectric layer for forming the second spacer, the deposition condition of the dielectric layer is suitable for performing the re-crystallization process on the amorphized material and the activation of the dopants in doped region (page 9, paragraph [0027] and page 12, paragraph [0036]).

However, Wieczorek et al. do not teach or suggest that the formation of the spacer, the re-crystallization of the amorphized material and the activation of the source/drain extension region can be performed in an identical process. Even though Wieczorek et al. do mention forming the amorphized source/drain extension region in the substrate and describe the details of re-crystallization, they still lack to imply that re-crystallization can be performed together with the formation of the spacer. Further, in paragraph 0048 in the citation, Wieczorek et al. mention that the spacers 12, 13 may remain on the substrate during the formation of the amorphized regions 14, 15. Additionally, another embodiment mentioned by Wieczorek et al. in paragraph 0049 states that the spacers 12, 13 are removed before the formation of the amorphized regions 14, 15. Hence, it is obvious that Wieczorek et al. never consider combining the formation of the spacers and the re-crystallization process. Therefore, people skilled in the art may not modify the cited reference to achieve the result of the present invention.

For at least the foregoing reasons, Applicants respectfully submits that independent claims 1, 8 and 14 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 5-7, 12-13, 21-22 and 24-31 patently define over the prior art as well.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1, 5-8, 12-14, 21-22 and 24-31 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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Date: 11/30/2004

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